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D/A CONVERTER

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[There are no amendments to this patent.]

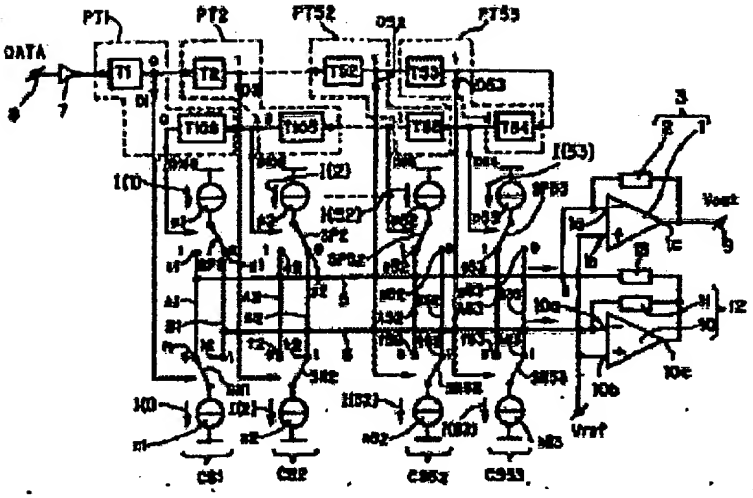
Abstract

Objective

To provide a small D/A converter at low cost.

Means to solve

Current source pairs CS1-CS53 are used corresponding to delay elements PT1-PT53.



Claims

1. A D/A converter characterized in that it comprises a plurality of delay elements that output serially input digital data as parallel data, two current sources used corresponding to two of the aforementioned delay elements, an analog data generating means that has two input parts connected to the aforementioned two current sources, respectively, and generates analog data from the currents input into the aforementioned two input parts, and a switching means that switches between a first mode, in which the aforementioned two current sources are connected to different input parts of the aforementioned two input parts based on the two data output from the aforementioned two delay elements, and a second mode, in which the aforementioned two current sources are connected to the same input part.

2. A D/A converter characterized in that it comprises a plurality of delay elements that output serially input digital data as parallel data, two current sources used corresponding to two of the aforementioned delay elements, an analog data generating means that has two input parts connected to the aforementioned two current sources, respectively, and generates analog data from the currents input into the aforementioned two input parts, and a switching means that switches between a third mode, in which the aforementioned two current sources are connected to different input parts of the aforementioned two input parts based on the two data output from the aforementioned two delay elements, and a fourth mode, in which the aforementioned two current sources are cut off from the aforementioned two input parts.

3. The D/A converter described in Claim 1 characterized in that the aforementioned switching means has a first switching part, which switches the connection between one of the aforementioned two current sources and each of the aforementioned two input parts based on one data output from one of the aforementioned two delay elements, and a second switching part,

which switches the connection between the other one of the aforementioned two current sources and each of the aforementioned two input parts based on one data output from the other one of the aforementioned two current sources.

4. The D/A converter described in Claim 2 characterized in that the aforementioned switching means has a third switching part, which switches the connection and disconnection between one of the aforementioned two current sources and the aforementioned two input parts based on the two data outputs from the aforementioned two delay elements, and a fourth switching part, which switches the connection and disconnection between the other one of the aforementioned two current sources and the aforementioned two input parts based on the aforementioned two data.

5. The D/A converter described in Claim 1 or 2 characterized in that the aforementioned two current sources supply currents of the same magnitude.

6. The D/A converter described in Claim 1 or 2 characterized in that the aforementioned analog data generating means has a sign changing means, which converts the current input into one of the aforementioned two input parts into a current of opposite sign, and a current/voltage converting means, which converts the sum of the current input into the other one of the aforementioned two input parts and the current whose sign has been changed by the aforementioned sign changing means into a voltage.

Detailed explanation of the invention

[0001]

Industrial application field

The present invention pertains to a D/A converter which contains current sources.

[0002]

Prior art

Figure 6 is a diagram illustrating a D/A converter having a 106-tap FIR filter as an example of the conventional D/A converter.

[0003]

This D/A converter has digital input terminal 8. Said digital input terminal 8 is connected to 106 delay elements T1-T106 connected in series via inverting amplifier 7. 1-bit data of either '0' or '1' is input in series and sequentially from digital input terminal 8 into delay element T1 via inverting amplifier 7. The data input into delay element T1 is transferred sequentially to the last delay element T106. In this case, the 106 delay elements T1-T106 not only output the data input in series into delay element T1 to the next delay element but also output the data as parallel

time-series data D1-D106. Data D1-D106 are sent to switches SP1, SN1 ; - ; SP106, SN106 to be explained below. This D/A converter has current source pairs CS1-CS106 comprised of two current sources p1 and n1, etc., corresponding to delay elements T1-T106. Each of said current source pairs CS1-CS106 is comprised of two current sources p1, n1 ; - ; p106, n106. These current sources generate currents corresponding to the amount (weighting amount) of weighting data D1-D106 output from delay elements T1-T106. Current sources p1, n1 ; - ; p106, n106 generate currents I(1)-I(106) of positive direction indicated by the arrow on the side of each current source in Figure 6.

[0004]

Figure 7 is a diagram illustrating the current generated by each current source.

[0005]

The abscissa of the diagram represents each current source p1, n1 ; - ; p106, n106, while the ordinate represents the current generated by each current source.

[0006]

The two current sources that constitute each of current source pairs CS1-CS106 generate identical currents. For example, as far as current source pair CS1 is concerned, two current sources p1 and n1 generate current I(1) (see Figures 6, 7). For other current source pairs CS2, .., CS105, CS106, two current sources p2, n2 ; .. ; p105, n105; p106, n106 generate currents I(2), ..., I(105), I(106), respectively.

[0007]

Also, these currents I(1)-I(106) satisfy the relationship of I(n) = I(107-n) (wherein, $1 \leq n \leq 53$, n is an integer). For example, when n = 1, I(1) = I(106). Consequently, the magnitudes of currents I(1)-I(106) shown in Figure 7 are symmetrical with respect to the current generated by current source pairs CS53 and CS54.

[0008]

The explanation based on Figure 6 is continued.

[0009]

This D/A converter has I/V converter 3 and dump buffer 4. Said I/V converter 3 has amplifier 1 and resistor 2. The two ends of resistor 2 are connected to the input terminal 1a and output terminal 1c of amplifier 1. On the other hand, input terminal 4a, out of the two input

terminals 4a and 4b of dump buffer 4, is connected to output terminal 4c. The other input terminal 4b is connected to the input terminal 1b of the amplifier 1 of I/V converter 3.

[0010]

This D/A converter also has two connecting wires A1, B1; -; A106, B106 corresponding to each of current source pairs CS1-CS106. The input terminal 1a of amplifier 1 of I/V converter 3 is connected to connecting wires A1-A106 out of two connecting wires A1, B1; -; A106, B106 via current path 5. On the other hand, the input terminal 4a of dump buffer 4 is connected to connecting wires B1-B106 via current path 6.

[0011]

Two switches SP1, SN1; -; SP106, SN106 used corresponding to each of current source pairs CS1-CS106 switch the connection between each of current sources p1, n1; -; p106, n106 and each two connecting wires A1, B1; - A106, B106 corresponding to the data D1-D106 output from delay elements T1-T106. By switching the connection, each current source is connected to I/V converter 3 or dump amplifier 4. Out of I/V converter 3 and dump amplifier 4, dump amplifier 4 does not convert digital data into analog data. Only I/V converter 3 converts the digital data into analog data. Consequently, only the current generated by the current source connected to I/V converter 3 is converted to voltage by I/V converter 3, and analog signal is output from analog output terminal 9.

[0012]

Problems to be solved by the invention

The aforementioned D/A converter is required to have current source pairs CS1-CS106 corresponding to 106 delay elements T1-T106. In other words, it is necessary to use 106 current sources p1-p106 and 106 current sources n1-n106 corresponding to 106 delay elements T1-T106. As a result, the cost becomes high, and the size of the D/A converter is increased.

[0013]

The purpose of the present invention is to solve the aforementioned problem by providing a small D/A converter at low cost.

[0014]

Means for solving the problems

The first D/A converter of the present invention for realizing the aforementioned purpose is characterized in that it comprises a plurality of delay elements that output serially input digital

data as parallel data, two current sources used corresponding to two of the aforementioned delay elements, an analog data generating means that has two input parts connected to the aforementioned two current sources, respectively, and generates analog data from the currents input into the aforementioned two input parts, and a switching means that switches between a first mode, in which the aforementioned two current source are connected to different input parts of the aforementioned two input parts based on the two data output from the aforementioned two delay elements, and a second mode, in which the aforementioned two current sources are connected to the same input part.

[0015]

In the first D/A converter of the present invention, two current sources are used corresponding to two delay elements. The switching means switches the connection between the aforementioned two current sources and each of the input parts of the analog data generating means corresponding to the two data output from the aforementioned two delay elements. Consequently, compared with the D/A converter using two current sources for one delay element, the first D/A converter of the present invention can reduce the number of current sources so that the cost and the size can be reduced.

[0016]

For the first D/A converter of the present invention, it is preferred that the aforementioned switching means contains a first switching part, which switches the connection between one of the aforementioned two current sources and each of the aforementioned two input parts based on one data output from one of the aforementioned two delay elements, and a second switching part, which switches the connection between the other one of the aforementioned two current sources and each of the aforementioned two input parts based on one data output from the other one of the aforementioned two current sources.

[0017]

By using the first and second switching parts, the connection between each of the two delay elements and each of the two current sources can be switched based on the two data output from the two delay elements.

[0018]

The second D/A converter of the present invention for realizing the aforementioned purpose is characterized in that it comprises a plurality of delay elements that output serially input digital data as parallel data, two current sources used corresponding to two of the

aforementioned delay elements, an analog data generating means that has two input parts connected to the aforementioned two current sources, respectively, and generates analog data from the currents input into the aforementioned two input parts, and a switching means that switches between a third mode, in which the aforementioned two current sources are connected to different input parts of the aforementioned two input parts based on the two data output from the aforementioned two delay elements, and a fourth mode, in which the aforementioned two current sources are cut off from the aforementioned two input parts.

[0019]

In the second D/A converter of the present invention, two current sources are used corresponding to two delay elements. The switching means switches the connection and disconnection between the two current sources and the input parts of the analog data generating means corresponding to the two data output from the aforementioned two delay elements. Consequently, compared with the D/A converter using two current sources for one delay element, the second D/A converter of the present invention can reduce the number of current sources so that the cost and the size can be reduced.

[0020]

For the second D/A converter of the present invention, it is preferred that the aforementioned switching means contains a third switching part, which switches connection and cutoff between one of the aforementioned two current sources and the aforementioned two input parts based on the two data outputs from the aforementioned two delay elements, and a fourth switching part, which switches the connection and cutoff between the other one of the aforementioned two current sources and the aforementioned two input parts based on the aforementioned two data.

[0021]

By using the third and fourth switching parts, the connection and disconnection between the other one of the aforementioned two current sources and the aforementioned two input parts can be switched based on the aforementioned two data.

[0022]

Also, for the first and second D/A converters of the present invention, it is preferred that the aforementioned two current sources supply currents of the same magnitude.

[0023]

For the first and second D/A converters of the present invention, it is preferred that the aforementioned analog data generating means have a sign changing means, which converts the current input into one of the aforementioned two input parts into a current of opposite sign, and a current/voltage converting means, which converts the sum of the current input into the other one of the aforementioned two input parts and the current with its sign changed by the aforementioned sign changing means to a voltage.

[0024]

By using the sign changing means and the current/voltage converting means, even if the directions of the currents flowing to the two input parts are opposite to each other, the directions of these currents can be made consistent so that the currents can be converted into a voltage.

[0025]

Embodiment

In the following, an embodiment of the present invention will be explained.

[0026]

Figure 1 is a diagram illustrating the D/A converter disclosed in an embodiment of the first D/A converter of the present invention.

[0027]

This D/A converter has digital input terminal 8. Said digital input terminal 8 is connected to 106 delay elements T1-T106 connected in series via inverting amplifier 7. 1-bit data of either '0' or '1' is input in series and sequentially from digital input terminal 8 into delay element T1 via inverting amplifier 7. The data input into delay element T1 is transferred sequentially to the last delay element T106. In this case, the 106 delay elements T1-T106 not only output the data input in series into delay element T1 to the next delay element but also output the data as parallel time-series data D1-D106. Data D1-D106 are sent to switches SP1, SN1 ; - ; SP53, SN53 to be explained below. This D/A converter has 53 current source pairs CS1-CS53 comprised of two current sources corresponding to delay element pairs PT1-PT53 comprised of two delay elements. In this case, delay element pair PTn is comprised of two delay elements Tn and T(107-n) (wherein, $1 \leq n \leq 53$, n is an integer). Also, each of current source pairs CS1-CS53 is comprised of two current sources p1, n1; -; p53, n53. The currents generated by current sources p1, n1; -; p53, n53 are the same as the currents generated by current sources p1, n1; -; p53, n53 shown in Figure 7, respectively.

[0028]

This D/A converter also has two connecting wires A1, B1; -; A53, B53 corresponding to current source pairs CS1-CS53. Each of current sources p1, n1; -; p53, n53 is connected in a switchable manner to two connecting wires A1, B1; -; A53, B53 by using respective switches SP1, SN1; ... SP53, SN53.

[0029]

This D/A converter has I/V converter 3 with the same configuration as I/V converter 3 shown in Figure 6. In addition to said I/V converter 3, the converter contains I/V converter 12. Said I/V converter 12 has amplifier 10 and resistor 11. The two ends of resistor 11 are connected to the input terminal 10a and output terminal 10c of amplifier 10. The input terminal 1a of I/V converter 3 and the output terminal 10c of I/V converter 12 are connected to each other via resistor 13. Also, the input terminal 1b of I/V converter 3 is connected to the input terminal 10b of I/V converter 12. The input terminal 1a of I/V converter 3 is connected to one connecting wire A1-A53 of two connecting wires A1, B1; -; A53, B53 corresponding to current source pairs CS1-CS53 via current path 5. Also, the input terminal 10a of I/V converter 12 is connected to the other connecting wire B1-B53 of two connecting wires A1, B1; -; A53, B53 via current path 6.

[0030]

As described above, this D/A converter has two switches SP1, SN1; ... SP53, SN53 corresponding to each of current source pairs CS1-CS53. These two switches SP1, SN1; ... SP53, SN53 switch the connection between the two current sources that constitute the corresponding current source pair CS1-CS53 and either one of the two connecting wires A1, B1; -; A53, B53 corresponding to the data output from the two delay elements T1, T106; -; T53, T54 that constitute delay element pairs PT1-PT53. In the following, the case when the connection of current source pairs CS1-CS53 is switched by two switches SP1, SN1; ...; SP53, SN53 will be explained in detail.

[0031]

Since the case when the connection of current source pairs CS1-CS53 is switched by two switches SP1, SN1; ...; SP53, SN53 can be explained in the same way as for any current source pair among current source pairs CS1-CS53, current source pair CS1 will be used as an example, and the case when the connection of current source pair CS1 is switched by two switches SP1, SN1 will be explained.

[0032]

When the data output from two delay elements T1 and T106 that constitute delay element pair PT1 are '0', switch SP1 is connected to the terminal g1 of connecting wire B1, while the other switch SN1 is connected to the terminal f1 of connecting wire A1 (equivalent to the first mode in the present invention). As a result, current source p1 of current source pair CS1 is connected to the input terminal 10a of I/V converter 12, while current source n1 is connected to the input terminal 1a of I/V converter 3. When the data output from two delay elements T1, T106 are both '1', the connections of switches SP1 and SN1 are switched such that switch SP1 is connected to the terminal e1 of connecting wire A1, while switch SN1 is connected to the terminal h1 of connecting wire B1 (equivalent to the first mode in the present invention). As a result, current source p1 is connected to the input terminal 1a of I/V converter 3, while current source n1 is connected to the input terminal 10a of I/V converter 12. If one of the data output from two delay elements T1, T106 is '0' and the other is '1', switches SP1 and SN1 are connected to each other (equivalent to the second mode in the present invention). More specifically, if the data output from delay element T1 is '0' and the data output from delay element T106 is '1', switches SP1 and SN1 are connected to connecting wire A1. On the other hand, if the data output from delay element T1 is '1' and the data output from delay element T106 is '0', switches SP1 and SN1 are connected to connecting wire B1. Other two switches SP2, SN2; -; SP53, SN53 operate in the same way as switches SP1 and SN1 corresponding to the data output from the corresponding two delay elements.

[0033]

For the analog data obtained by inputting digital data into the D/A converter shown in Figure 1 with the aforementioned configuration and the analog data obtained by inputting digital data into the conventional D/A converter shown in Figure 6, if the input digital data are the same, the same analog data will be output. The case in which the D/A converters shown in Figures 1 and 6 output the same analog data will be explained below.

[0034]

When 1-bit data of '0' or '1' is input in series and sequentially into delay element T1 in the D/A converter shown in Figure 1, each of delay elements T1-T106 outputs the data to the next delay element. In this case, the 106 delay elements T1-T106 not only output the data to the next delay element but also output parallel time-series data D1-D106. Two switches SP1, SN1; SP2, SN2; ...; SP52, SN52; SP53, SN53 used corresponding to the current source pairs operate such that each current source is connected to either I/V converter of I/V converters 3 or 12 corresponding to the data output from the two delay elements T1, T106; T2, T105; -; T52, T55,

T53, T54 that constitute the delay element pairs. In this case, the operation of delay element pair PT1 of delay element pairs PT1-PT53 will be explained. If the data output from two delay elements T1 and T106 that constitute said delay element pair PT1 are '0' and '0', current source p1 is connected to the terminal g1 of connecting wire B1, while current source n1 is connected to the terminal f1 of connecting wire A1. Consequently, current source n1 is connected to the input terminal 1a of I/V converter 3, while current source p1 is connected to the input terminal 10a of I/V converter 12. As a result, negative current –I(1) flows from current source n1 through current path 5 to the connection point C between resistor 13 and the input terminal 1a of I/V converter 3. On the other hand, positive current I(1) flows from current source p1 to the input terminal 10a of I/V converter 12. The positive current I(1) is converted into a voltage by I/V converter 12. Since I/V converter 12 is an inverting circuit, a negative voltage is generated at the output terminal 10c of I/V converter 12. The negative voltage generated at output terminal 10c is converted into a current by resistor 13 and is transferred to the connection point C between resistor 13 and the input terminal 1a of I/V converter 3. As a result, when current source p1 is connected to I/V converter 12, negative current –I(1) obtained by inverting the sign of positive current I(1) flows from current source p1 to connection point C. Consequently, when current sources p1 and n1 are connected to I/V converters 12 and 3, negative current –I(1) flows from current sources p1 and n1 to connection point C. Negative current –I(1) generated by current source p1 and negative current -I(1) generated by current source n1 are added at connection point C. Therefore, the current –I(1)-I(1)= -2I(1) flows to the input terminal 1a of I/V converter 3. A voltage corresponding to –2I(1) is generated at analog output terminal 9.

[0035]

If the data output from two delay elements T1 and T106 are '1' and '1', current source p1 is connected to the terminal e1 of connecting wire A1, while current source n1 is connected to the terminal h1 of connecting terminal B1. Consequently, current source p1 is connected to the input terminal 1a of I/V converter 3, while current source n1 is connected to the input terminal 10a of I/V converter 12. As a result, positive current I(1) flows from current source p1 to connection point C. On the other hand, negative current –I(1) flows from current source n1 to the input terminal 10a of I/V converter 12. The negative current –I(1) is converted into a voltage by I/V converter 12. Since I/V converter 12 is an inverting circuit, a positive voltage is generated at the output terminal 10c of I/V converter 12. As a result, positive current I(1) flows to connection point C by connecting current source n1 to I/V converter 12. The positive voltage generated at output terminal 10c is converted to a current by resistor 13 and is sent to connection point C. As a result, when current source n1 is connected to I/V converter 12, a positive current I(1) flows to connection point C. Consequently, when current sources p1 and n1 are connected to I/V

converters 3 and 12, positive current I(1) flows from each of current sources p1 and n1 to connection point C. The positive current I(1) generated by current source p1 and the positive current I(1) generated by current source n1 are added at connection point C. Therefore, the current I(1) + I(1) = 2I(1) flows to the input terminal 1a of I/V converter 3. A voltage corresponding to 2I(1) is generated at analog output terminal 9.

[0036]

If the data output from two delay elements T1 and T106 are '0' and '1' (or '1' and '0'), current sources p1 and n1 are connected to each other. Consequently, in this case, the current I(1) generated by current source p1 and the current I(1) generated by current source n1 cancel each other out. As a result, a voltage corresponding to zero current is generated at analog output terminal 9.

[0037]

To summarize what has been described above, when the data combination is '0' and '0', a voltage corresponding to -2I(1) is generated at analog output terminal 9 by current sources p1 and n1. When the data combination is '1' and '1', a voltage corresponding to 2I(1) is generated at analog terminal 9 by current sources p1 and n1. Also, if the data output from two delay elements T1 and T106 are '0' and '1' (or '1' and '0'), a voltage corresponding to zero current is generated at analog output terminal 9 by current sources p1 and n1.

[0038]

In the following the conventional D/A converter shown in Figure 6 will be explained for the case when the data output from two delay elements T1 and T106 change sequentially as '0' and '0', '1' and '1', '0' and '1' (or '1' and '0'), like the D/A converter shown in Figure 1.

[0039]

If the data output from two delay elements T1 and T106 shown in Figure 6 are '0' and '0', current sources p1 and n1 are connected to the terminal g1 of connecting wire B1 and the terminal f1 of connecting wire A1, respectively. Current sources p106 and n106 are connected to the terminal g106 of connecting wire B106 and the terminal f106 of connecting wire A106, respectively. Consequently, in this case, of current sources p1, n1, p106, and n106, current sources p1 and p106 are connected to dump buffer 4. As described above, dump buffer 4 makes no contribution to converting the digital data into analog data. Consequently, two current sources, that is, n1 and n106 of the four current sources p1, n1, p106, and n106 are connected to I/V converter 3, which makes contribution to converting the digital data into analog data. When

two current sources n1 and n106 are connected to I/V converter 3, negative current –I(1) and -I(106) flow from two current sources, that is, n1 and n106 to I/V converter 3, respectively. Consequently, the current –I(1)-I(106) flows into the input terminal 1a of I/V converter 3. A voltage corresponding to the current of –I(1)-I(106) is generated at analog output terminal 9. As explained above based on Figure 7, since current I(1) and current I(106) are equal to each other,

[0040]

$I(1) = I(106)$ ... (1)

$-I(1) - I(106) = -I(1) - I(1) = -2I(1)$. A voltage corresponding to the current of $-2I(1)$ is generated at analog output terminal 9. If the data output from two delay elements T1 and T106 are '0' and '0', the D/A converter shown in Figure 6 generates a voltage corresponding to a current of $-2I(1)$ is generated at analog output terminal 9 in the same way as the D/A converter shown in Figure 1.

[0041]

Then, for the D/A converter shown in Figure 6, if the data output from two delay elements T1 and T106 are '1' and '1', current sources p1 and n1 are connected to the terminal e1 of connecting wire A1 and the terminal h1 of connecting wire B1, respectively. Current sources p106 and n106 are connected to the terminal e106 of connecting wire A106 and the terminal h106 of connecting wire B106, respectively. Consequently, in this case, two current sources, that is, p1 and p106 of the four current sources p1, n1, p106, and n106 are connected to I/V converter 3. When two current sources p1 and p106 are connected to I/V converter 3, positive current I(1) and I(106) flow from said two current sources p1 and p106 to I/V converter 3, respectively. Consequently, the current $I(1) + I(106)$ flows to the input terminal 1a of I/V converter 3. A voltage corresponding to the current of $I(1) + I(106)$ is generated at analog output terminal 9. As explained above based on Figure 7, since current I(1) and current I(106) are equal to each other, based on equation (1), $I(1) + I(106) = I(1) + I(1) = 2I(1)$. A voltage corresponding to $2I(1)$ is generated at analog output terminal 9. That is, when the data output from two delay elements T1 and T106 are '1' and '1', the D/A converter shown in Figure 6 generates a voltage corresponding to a current of $2I(1)$ at analog output terminal 9 in the same way as the D/A converter shown in Figure 1.

[0042]

Then, for the D/A converter shown in Figure 6, if the data output from delay element T1 is '0' and the data output from delay element T106 is '1', current sources p1 and n1 are connected to the terminal g1 of connecting wire B1 and the terminal f1 of connecting wire A1, respectively.

Current sources p106 and n106 are connected to the terminal e106 of connecting wire A106 and the terminal h106 of connecting wire B106, respectively. Consequently, in this case, two current sources, that is, n1 and p106 among the four current sources p1, n1, p106, and n106 are connected to I/V converter 3. When two current sources n1 and p106 are connected to I/V converter 3, current –I(1) and I(106) flow from said two current sources n1 and p106 to I/V converter 3, respectively. Consequently, the current–I(1) + I(106) flows to the input terminal 1a of I/V converter 3. As explained above based on Figure 7, current I(1) and current I(106) are equal. Consequently, based on equation (1), -I(1) + I(106) = -I(1) + I(1) = 0, the currents generated by two current sources n1 and p106 cancel each other out. Consequently, a voltage corresponding to zero current is generated at analog output terminal 9. The situation is the same when the data output from delay element T1 is '1' and the data output from delay element T106 is '0'. In other words, a voltage corresponding to zero current is generated at analog output terminal 9. In summary, when the data output from two delay elements T1 and T106 are '0' and '1' (or '1' and '0'), the D/A converter shown in Figure 6 generates a voltage corresponding to zero current at analog output terminal 9 in the same way as the D/A converter shown in Figure 1.

[0043]

To summarize what has been described above, for both D/A converters shown in Figures 1 and 6, when the data output from two delay elements T1 and T106 are '0' and '0', a voltage corresponding to –2I(1) is generated at analog output terminal 9. When the data are '1' and '1', a voltage corresponding to 2I(1) is generated at analog output terminal 9. When the data output from two delay elements T1 and T106 are '0' and '1' (or '1' and '0'), a voltage corresponding to zero current is generated at analog output terminal 9.

[0044]

In other words, for the voltage generated at analog output terminal 9, the voltages generated by data D1 and D106 output from two delay elements T1 and T106 are equal to each other for the D/A converters shown in Figures 1 and 6. Similarly, for the voltage generated at analog output terminal 9, the voltages generated by the data output from two delay elements T2, T105; -; T53, T54 are equal to each other for the D/A converters shown in Figures 1 and 6. Consequently, the D/A converters shown in Figures 1 and 6 output the same analog data.

[0045]

Here, two current sources p1 and n1 will be explained. For the D/A converter shown in Figure 1, if the data output from delay elements T1 and T106 are '0' and '0' or '1' and '1', as described above, one of two current sources p1 and n1 is connected to current path 5, while the

other current source is connected to current path 6. The current flowing in current path 6 is converted into a current with its sign inverted by I/V converter 12 and resistor 13 and is added to the current flowing through current path 5 at connection point C. Consequently, both the current generated by current source p1 and the current generated by current source n1 flow to the input terminal 1a of I/V converter 3. On the other hand, for the conventional D/A converter shown in Figure 6, as explained above, only one of the currents generated by current source p1 or by current source n1 flows to I/V converter 3. Therefore, the current flowing to the input terminal 1a of I/V converter 3 comprised of two current sources p1 and n1 in the D/A converter shown in Figure 1 is twice that of the conventional D/A converter shown in Figure 6. As far as the D/A converter shown in Figure 6 is concerned, since current source pair CS106 used corresponding to delay element T106 conducts the same weighting as current source pair CS1 with respect to data D106 output from delay element T106 (see Figure 7), current source pair CS106 sources a current equal to that of current source pair CS1 to the input terminal 1a of I/V converter 3. In other words, current source CS1 in the D/A converter shown in Figure 1 sources a current obtained by combining those of current sources CS1 and CS106, which perform equal weighting in the D/A converter shown in Figure 6, to the input terminal 1a of I/V converter 3. Similarly, current source CSn ($1 \leq n \leq 53$, n is an integer) in the D/A converter shown in Figure 1 sources a current obtained by combining those of current sources CSn and CS(107-n) ($1 \leq n \leq 53$, n is an integer), which perform equal weighting in the D/A converter shown in Figure 6, to I/V converter 3.

[0046]

As described above, the D/A converter shown in Figure 1 focuses on the fact that current source pairs CSn and CS(107 - n) in the conventional D/A converter shown in Figure 6 execute equal weighting. The D/A converter shown in Figure 1 has a configuration such that the currents of the two current sources that constitute a current source pair are added at connection point C corresponding to the combination of data output from two delay elements. When the D/A converter shown in Figure 1 adopts the aforementioned configuration, the D/A converter shown in Figure 1 can reduce the number of current sources required for the D/A converter while keeping the function of the conventional D/A converter shown in Figure 6. More specifically, in the D/A converter shown in Figure 6, since a group of current source pairs is used corresponding to one delay element, the number of required current sources is a total of 212. On the other hand, in the D/A converter shown in Figure 1, since one group of current source pairs is used corresponding to one group of delay element pairs (two delay elements), only 106 current sources are needed. Consequently, the D/A converter shown in Figure 1 can realize the same function as that of the D/A converter shown in Figure 6 by using half of the current sources.

Therefore, the cost can be cut. Also, since the number of current sources can be reduced by half, the chip area required for mounting the D/A converter can be significantly reduced so that the D/A converter can be miniaturized.

[0047]

In Figure 1, of two switches SP1, SN1; -; SP53, SN53, switches SP1-SP53 correspond to the first switching part mentioned in the present invention, while switches SN1-SN53 correspond to the second switching part mentioned in the present invention. Also, the combination of I/V converter 12 and resistor 13 is equivalent to the sign changing means mentioned in the claims of the present invention. I/V converter 3 is equivalent to the current/voltage converting means mentioned in the claims of the present invention.

[0048]

Figure 2 is a diagram illustrating the D/A converter disclosed in the first embodiment of the second D/A converter of the present invention.

[0049]

For explanation of the D/A converter shown in Figure 2, the same constituent parts as those of the D/A converter shown in Figure 1 are represented by the same respective symbols. Only the differences from the D/A converter shown in Figure 1 will be explained.

[0050]

There are two differences between the D/A converters shown in Figures 1 and 2.

[0051]

As far as the first difference is concerned, the D/A converter shown in Figure 1 has two connecting wires A1, B1; -; A53, B53 connected to current paths 5, 6 corresponding to current source pairs CS1-CS53, and two switches SP1, SN1; -; SP53, SN53 are used to switch the connection between each of two connecting wires A1, B1; -; A53, B53 and the current sources. On the other hand, the D/A converter shown in Figure 2 has connecting wires C1-C53 disconnected from current paths 5, 6 in addition to two connecting wires A1, B1; -; A53, B53 connected to current paths 5, 6, and two switches SP1, SN1; -; SP53, SN53 are used to switch the connection between each of three connecting wires A1, B1, C1; -; A53, B53, C53 and the current sources.

[0052]

As far as the second difference is concerned, in the D/A converter shown in Figure 1, each of two switches SP1, SN1; -; SP53, SN53 switches the connection of the corresponding current source pair corresponding to one data output from one delay element. In the D/A converter shown in Figure 2, however, two switches SP1, SN1; -; SP53, SN53 switch the connection of the corresponding current source pair corresponding to two data output from two delay elements T1, T106; -;T53, T54. In the following, the D/A converter shown in Figure 2 will be explained in detail in the case when connection of current source pairs CS1-CS53 is switched by two switches SP1, SN1; ...; SP53, SN53.

[0053]

Since the case when the connection of current source pairs CS1-CS53 is switched by two switches SP1, SN1; ...; SP53, SN53 can be explained in the same way as for any current source pair of current source pairs CS1-CS53, current source pair CS1 will be used as an example, and the case when the connection of current source pair CS1 is switched by two switches SP, SN1 will be explained.

[0054]

When the data output from two delay elements T1 and T106 that constitute delay element pair PT1 are both '0' (that is, when the data output from two delay elements T1 and T106 are '0' and '0'), switch SP1 is connected to the terminal g1 of connecting wire B1, while the other switch SN1 is connected to the terminal f1 of connecting wire A1 (equivalent to the third mode mentioned in the present invention). As a result, current source p1 of current source pair CS1 is connected to the input terminal 10a of I/V converter 12, while current source n1 is connected to the input terminal 1a of I/V converter 3. When the data output from two delay elements T1, T106 are both '1' (that is, when the data output from two delay elements T1 and T106 are '1' and '1'), the connections of switches SP1 and SN1 are switched such that switch SP1 is connected to the terminal e1 of connecting wire A1, while switch SN1 is connected to the terminal h1 of connecting wire B1 (equivalent to the third mode mentioned in the present invention). As a result, current source p1 is connected to the input terminal 1a of I/V converter 3, while current source n1 is connected to the input terminal 10a of I/V converter 12. When one of the data output from two delay elements T1, T106 is '0' and the other data is '1', the connections of switches SP1 and SN1 are switched such that switch SP1 is connected to the terminal j1 of connecting wire C1, while switch SN1 is connected to the terminal k1 of connecting wire C1 (equivalent to the fourth mode mentioned in the present invention). Other two switches SP2, SN2; -;SP53, SN53

operate in the same way a switches SP1 and SN1 corresponding to the data output from the corresponding two delay elements.

[0055]

For the analog data obtained by inputting digital data into the D/A converter shown in Figure 2 with the aforementioned configuration and the analog data obtained by inputting digital data into the conventional D/A converter shown in Figure 6, if the digital data input are the same, the same analog data will be output. In the following, the case in which the D/A converters shown in Figures 2 and 6 output the same analog data will be explained.

[0056]

When 1-bit data of '0' or '1' is input in series and sequentially into delay element T1 in the D/A converter shown in Figure 2, each of delay elements T1-T106 outputs the data to the next delay element. In this case, the 106 delay elements T1-T106 not only output the data to the next delay element but also output parallel time-series data D1-D106. Two switches SP1, SN1; SP2, SN2; ...; SP52, SN52; SP53, SN53 used corresponding to the current source pairs operate such that each current source is connected to I/V converter 3 or 12, or is disconnected from I/V converters 3 and 12, corresponding to the data output from the two delay elements T1, T106; T2, T105; -; T52, T55, T53, T54 that constitute the delay element pairs. In this case, the operation of delay element pair PT1 of delay element pairs PT1-PT53 will be explained. If the data output from two delay elements T1 and T106 that constitute said delay element pair PT1 are '0' and '0', current source p1 is connected to the terminal g1 of connecting wire B1, while current source n1 is connected to the terminal f1 of connecting wire A1. Consequently, current source n1 is connected to the input terminal 1a of I/V converter 3, while current source p1 is connected to the input terminal 10a of I/V converter 12. As explained above, for the D/A converter shown in Figure 1, when the data output from two delay elements T1 and T106 are '0' and '0', current source n1 is connected to the input terminal 1a of I/V converter 3, while current source p1 is connected to the input terminal 10a of I/V converter 12. Consequently, for the D/A converter shown in Figure 2, when the data output from two delay elements T1 and T106 are '0' and '0', a voltage corresponding to a current of $-2I(1)$ is generated at analog output terminal 9 in the same way as the D/A converter shown in Figure 1.

[0057]

For the D/A converter shown in Figure 2, if the data output from two delay elements T1 and T106 are '1' and '1', current source p1 is connected to the terminal e1 of connecting wire A1, while current source n1 is connected to the terminal h1 of connecting terminal B1. Consequently,

current source p1 is connected to the input terminal 1a of I/V converter 3, while current source n1 is connected to the input terminal 10a of I/V converter 12. As explained above, for the D/A converter shown in Figure 1, when the data output from two delay elements T1 and T106 are '1' and '1', current source p1 is connected to the input terminal 1a of I/V converter 3, while current source n1 is connected to the input terminal 10a of I/V converter 12. Consequently, for the D/A converter shown in Figure 2, when the data output from two delay elements T1 and T106 are '1' and '1', a voltage corresponding to a current of 2I(1) is generated at analog output terminal 9 in the same way as the D/A converter shown in Figure 1.

[0058]

For the D/A converter shown in Figure 2, if the data output from two delay elements T1 and T106 are '0' and '1' (or '1' and '0'), current source p1 is connected to the terminal j1 of connecting wire C1, while current source n1 is connected to the terminal k1 of connecting wire C1. In other words, current sources p1 and n1 are connected to connecting wire C1 that is disconnected from current paths 5, 6. Consequently, in this case, no voltage corresponding to current sources p1 and n1 is generated at analog output terminal 9.

[0059]

To summarize what has been described above, when the data output from two delay elements T1 and T106 are '0' and '0', a voltage corresponding to -2I(1) is generated at analog output terminal 9 by current sources p1 and n1. When the data combination is '1' and '1', a voltage corresponding to 2I(1) is generated at analog terminal 9. Also, if the data output from two delay elements T1 and T106 are '0' and '1' (or '1' and '0'), a voltage corresponding to zero current is generated at analog output terminal 9.

[0060]

In other words, for the voltage generated at analog output terminal 9, the voltages generated by the data output from two delay elements T1 and T106 are equal to each other for the D/A converters shown in Figures 1 and 2. Similarly, for the voltage generated at analog output terminal 9, the voltages generated by the data output from two delay elements T2, T105; -; T53, T54 are equal for the D/A converters shown in Figures 1 and 2. As explained above, the voltage generated at analog output terminal 9 is the same for the D/A converter shown in Figure 1 and the conventional D/A converter shown in Figure 6. Consequently, the D/A converters shown in Figures 2 and 6 have the same function.

[0061]

Like the D/A converter shown in Figure 1, the D/A converter shown in Figure 2 also focuses on the fact that current source pairs CSn and CS(107-n) in the conventional D/A converter shown in Figure 6 execute equal weighting. The D/A converter shown in Figure 2 has a configuration such that the currents of the two current sources that constitute a current source pair are added at connection point C corresponding to the combination of data output from two delay elements. By adopting this configuration, it is possible to reduce the number of current sources required for the D/A converter while keeping the function of the conventional D/A converter shown in Figure 6. Like the D/A converter shown in Figure 1, the D/A converter shown in Figure 2 only requires 106 current sources. Consequently, the D/A converter shown in Figure 2 can realize the same function as that of the D/A converter shown in Figure 6 by using half of the current sources. Therefore, the cost can be reduced. Also, since the number of current sources can be reduced by half, the chip area required for mounting the D/A converter can be significantly reduced so that the D/A converter can be miniaturized.

[0062]

For both of the D/A converters shown in Figures 1, 2, current source pairs CS1-CS53 are prepared corresponding to two delay elements (delay element pair). However, there is no need to provide all of current source pairs CS1-CS53 corresponding to two delay elements (delay element pair). For example, any of current source pairs CS1-CS53 can be provided corresponding to two delay elements (delay element pair), while the rest of the current sources are prepared corresponding to one delay element. Even if the current source pairs prepared corresponding to two delay elements (delay element pair) and the current source pairs prepared corresponding to one delay element are both present, since any current source pair is prepared corresponding to the two delay elements (delay element pair), the number of current sources used can be reduced compared with the conventional technology, so that the cost can be reduced and miniaturization can be realized.

[0063]

Also, in Figure 2, of two switches SP1, SN1; -; SP5, SN53, switches SP1-SP53 correspond to the third switching part mentioned in the claims of the present invention. Switches SN1-SN53 correspond to the fourth switching part mentioned in the claims of the present invention.

[0064]

Figures 1 and 2 show examples of a D/A converter, which can reduce the cost while maintaining the same performance as that of the conventional D/A converter having an even number (106) of delay elements (see Figure 6). However, it is also possible to use an odd number of delay elements in the present invention. In the following, a D/A converter, which has the same function as a conventional D/A converter having an odd number of delay elements and is less costly than the conventional D/A converter having an odd number of delay elements, will be explained. In this case, first, the conventional D/A converter having 107 delay elements will be briefly explained with reference to Figure 6. Then, an example of the D/A converter of the present invention having the same function as the conventional D/A converter having 107 delay elements will be explained.

[0065]

When the conventional D/A converter shown in Figure 6 has, in addition to 106 delay elements T1-T106, delay element T107, in order to weight the data D107 output from delay element T107, it is necessary to use a current source pair CS107 comprised of two current sources p107 and n107. In other words, it is necessary to use 107 groups of current sources CS1-CS107.

[0066]

Figure 3 shows an example of the currents generated by said 107 groups of current source pairs CS1-CS107.

[0067]

The abscissa of the diagram represents current source pairs CS1-CS107, while the ordinate represents the current generated by each current source pair.

[0068]

The two current sources p1, n1; ...; p107, n107 that constitute each of current source pair CS1, ... CS107 generate equal currents I(1), ..., I(107). Also, as shown in Figure 3, of the currents I(1), ..., I(107) generated by current source pairs CS1-CS107, the current I(54) generated by current source pair CS54 is the largest.

[0069]

Also, these currents I(1), ..., I(107) satisfy the relationship of $I(n) = I(108-n)$ (wherein, $1 \leq n \leq 53$, n is an integer). For example, if $n = 1$, $I(1) = I(107)$. Consequently, the magnitudes of

currents I(1), ..., I(107) shown in Figure 3 are symmetrical with respect to the current I(54) generated by current source pair CS54.

[0070]

Figure 4 shows an example of the D/A converter of the present invention having the same function as the conventional D/A converter having current sources that generate currents as shown in Figure 3.

[0071]

Figure 4 shows the D/A converter disclosed in the second embodiment of the second D/A converter of the present invention.

[0072]

Only the difference between the D/A converter shown in Figure 4 and the D/A converter shown in Figure 2 will be briefly explained.

[0073]

The D/A converter shown in Figure 2 has 106 delay elements T1-T106 and 53 groups of current source pairs CS1-CS53, while the D/A converter shown in Figure 4 has 107 delay elements T1-T107 and 54 groups of current source pairs CS1-CS54. Of these 54 groups of current source pairs, 53 groups of current source pairs CS1-CS53 are prepared corresponding to delay element pairs PT1-PT53 comprised of two delay elements, while the remaining single group of current source pair CS54 is prepared corresponding to one delay element T54. Also, delay element pair PTn is comprised of two delay elements Tn and T(108-n) (wherein, $1 \leq n \leq 53$, n is an integer).

[0074]

Current sources p1, n1 ; - ; p54, n54 generate currents I(1)-I(154) with the positive direction indicated by the arrow on the side of each current source as shown in Figure 4. The two current sources of each of current source pairs CS1-CS54 generate equal currents. For example, as far as current source pair CS1 is concerned, both of the two current sources p1 and n1 generate current I(1). For other current source pairs CS2, ..., CS54, two current sources p2, n2; ...; p54, n54 generate equal currents I(2), ..., I(54).

[0075]

Also, each of two switches SP1, SN1; -; SP53, SN53 prepared corresponding to current source pairs CS1-CS53 among current source pairs CS1-CS54 switches the connection between each of current sources p1, n1; -; p53, n53 and three connecting wires A1, C1, B1; -; A53, C53, B53 corresponding to the combination of the two data D1, D107; - D53, D55 output from two delay elements T1, T107; -; T53, T55.

[0076]

Also, two connecting wires A54 and B54 and two stitches SP54 and SN54 are prepared corresponding to current source pair CS54. Said two connecting wires A54 and B54 are connected to current paths 5 and 6, respectively. Switch SP54 is used to switch the connection between current source p54 and two connecting wires A54 and B54 corresponding to the data D54 output from delay element T54. Switch SN54 is used to switch the connection between current source n54 and two connecting wires A54 and B54 corresponding to the data D54 output from delay element T54.

[0077]

The D/A converter shown in Figure 4 has 107 delay elements. In other words, the D/A converter shown in Figure 4 has an odd number of delay elements. Therefore, when 107 delay elements T1-T107 are divided into pairs comprised of two delay elements, one unpaired delay element remains. In the D/A converter shown in Figure 4, delay element T54 is not paired with other delay elements. Consequently, current source pair CS54 is prepared corresponding to this one delay element T54. In order for the D/A converter shown in Figure 4 to have the same performance as that of the conventional D/A converter having current sources that generate currents as shown in Figure 3, the currents generated by current source pairs CS1-CS54 shown in Figure 4 are set as shown in Figure 5.

[0078]

Figure 5 shows the current generated by each current source in Figure 4.

[0079]

The abscissa of the diagram represents each current source p1, n1 ; - ; p54, n54, while the ordinate represents the current generated by each current source.

[0080]

Of the currents I(1)-I(54) generated by current source pairs CS1-CS54 shown in Figure 5, currents I(1)-I(53) have the same magnitudes as the currents I(1)-I(53) generated by current source pairs CS1-CS53 shown in Figure 3, respectively. The current I(54) generated by current source pair CS54 shown in Figure 5 is half of the current I(54) generated by current source pair CS54 shown in Figure 3.

[0081]

By setting the current of each current source as shown in Figure 5, the same function as that of the D/A converter of Figure 4, which has the same function as the conventional D/A converter having current sources that generate the currents shown in Figure 3 can be realized.

[0082]

When the conventional D/A converter has 107 delay elements, it is necessary to use 107 groups of current source pairs (that is, 214 current sources) corresponding to these 107 delay elements. For the D/A converter shown in Figure 4, although current source pair CS54 is prepared corresponding to one delay element T54, the remaining current source pairs CS1-CS53 are prepared corresponding to delay element pairs PT1-PT53. Therefore, only 108 current sources are required. Consequently, by using the D/A converter shown in Figure 4, the same function as that of the conventional D/A converter can be realized, and the number of the required current sources can be reduced. Consequently, the cost can be reduced, and the size miniaturized.

[0083]

Effect of the invention

As explained above, according to the present invention, the cost of the D/A converter can be reduced, and the size miniaturized.

Brief explanation of the figures

Figure 1 is a diagram illustrating the D/A converter disclosed in an embodiment of the first D/A converter of the present invention.

Figure 2 is a diagram illustrating the D/A converter disclosed in the first embodiment of the second D/A converter of the present invention.

Figure 3 is a diagram illustrating an example of the currents generated by 107 groups of current source pairs CS1-CS107.

Figure 4 is a diagram illustrating the D/A converter disclosed in the second embodiment of the second D/A converter of the present invention.

Figure 5 is a diagram illustrating the current generated by each current source.

Figure 6 is a diagram illustrating a D/A converter having a 106-tap FIR filter as an example of the conventional D/A converter.

Figure 7 is a diagram illustrating the current generated by each current source.

Explanation of symbols

1, 10 Amplifiers

1a, 1b, 10a, 10b Input terminals

1c, 10c Output terminals

2, 11, 13 Resistors

3, 12 I/V Converters

5, 6 Current paths

7 Inverting amplifier

8 Digital input terminal

9 Analog output terminal

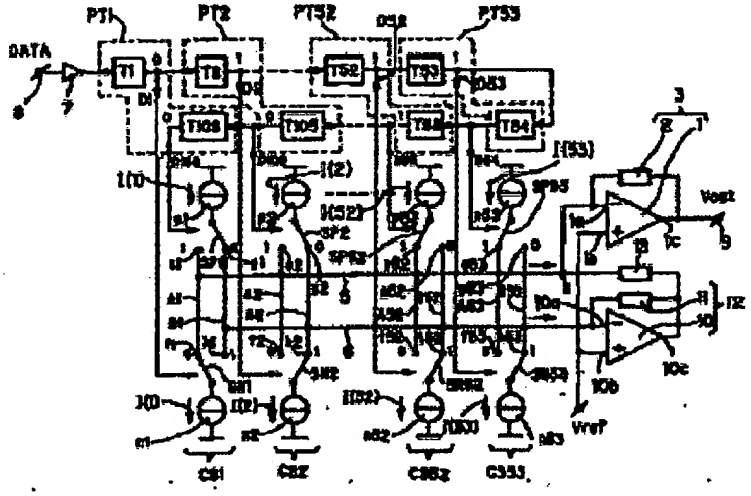


Figure 1

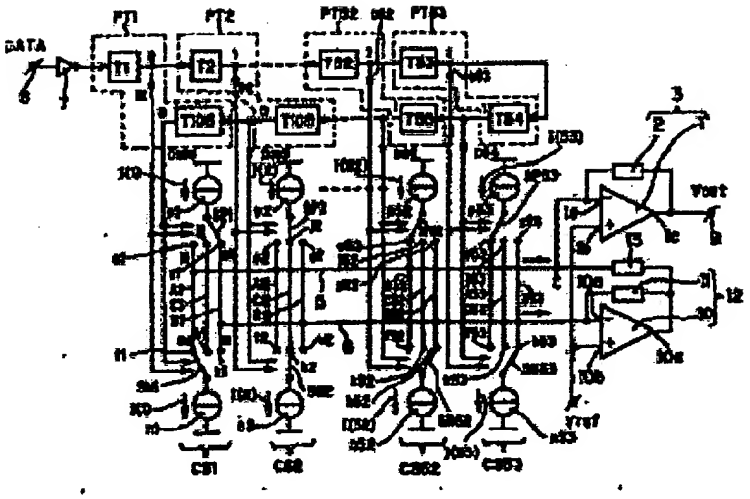


Figure 2

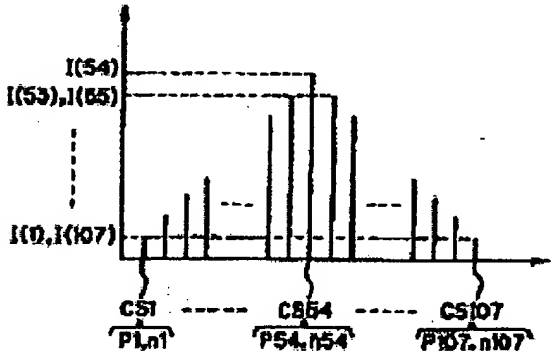


Figure 3

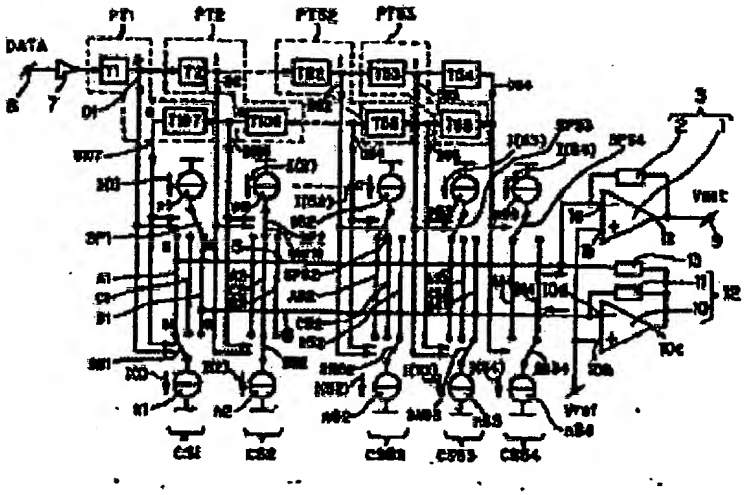


Figure 4

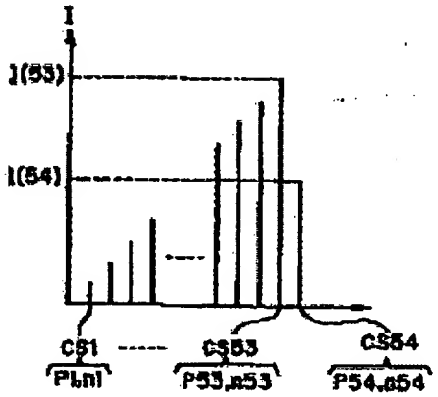


Figure 5

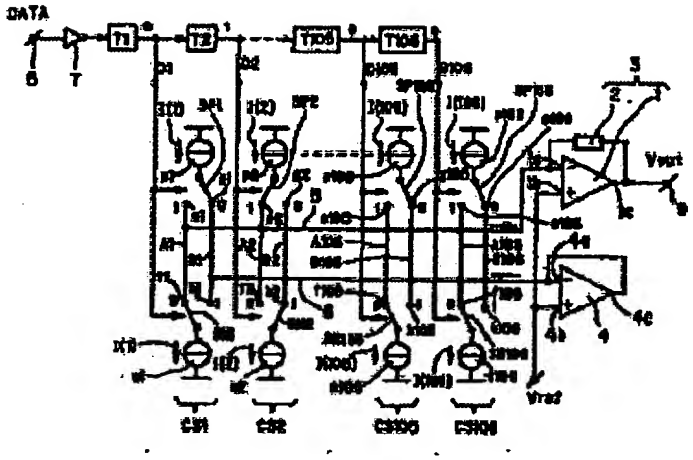


Figure 6

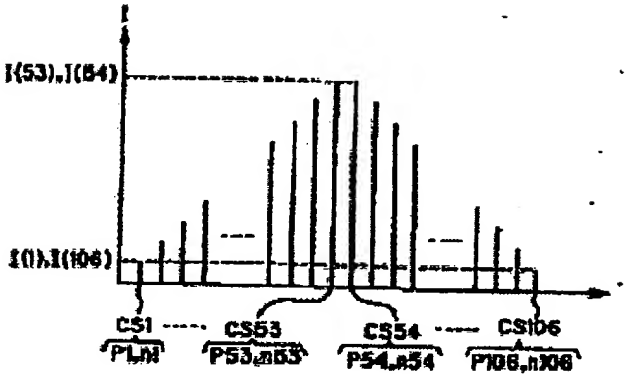


Figure 7

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